Set Items Description
S1 4799966 S (MEMORY OR MEMORIES OR RAM OR (RANDOM(1W)ACCESS(1W)MEMORY) OR EEPROM? ? OR READ(1N)WRITE OR DRAM? ? OR SDRAM? ? OR RDRAM? ? OR DIMM? ? OR SODIMM? ? OR ECC OR PRAM OR SIMM OR DATA()STORE OR DATA()STORAGE OR STORAGE OR READ()ONLY OR CACHE()STORAGE OR BUFFER OR HD OR HARD()DRIVE OR AREA OR LOCATION OR STORAGE OR COMPACTFLASH OR SMARTMEDIA OR MEMORY()STICK OR SD()MEMORY OR XD()PICTURE OR CARD OR USB()KEY OR STORAGE OR STORE OR CACHE OR EPROM? ? OR BUFFER? ? OR DISC? ? OR DISK? ?)
S2 42832 S S1(5N)(((SECOND OR 2ND OR TWO OR 2 OR MULTIPLE OR TWOFOLD OR DUAL OR PLURAL OR PLURALITY OR MULTIPLE? OR MULTI OR PAIR??)(2N)BUFFER? ?) OR GPU OR (GRAPHIC? ?(1W)PROCESS?(1W)UNIT? ?) OR COPROCESSOR? ? OR (COPROCESSOR? ?()READABLE))
S3 139 S S2(10N)(PAGING OR MAPP???)
S4 6688 S S1(5N)((PROPER OR CORRECT OR RIGHT OR MEET DECOROUS OR DISCREET? ? OR BELONG? FIT OR FITTING)(3N)(LOCATION? OR ADDRESS? ? OR SPACES? ? OR POSITION? ? OR REGION? ?))
S5 68854 S S1(5N)(INDICATOR? OR POINTER? ? OR INDEX? OR GAUGE OR BELLWETHER? ? OR DETECTOR? ?)
S6 139 S S2 AND S3
S7 10 S S6 AND S5
S8 10 S S7 AND PY=1963:2003

?

Subject summary

? t /3,k/all
8/3,K/1 (Item 1 from file: 350) Links
Fulltext available through: Order File History
Derwent WPIX

0013266697 & & *Drawing available*
WPI Acc no: 2003-352483/200333
XRPX Acc No: N2003-281519
Data buffer management method for data transfer between personal computer interface and local area network systems, involves converting data frame to specified format and updating pointer after transfer is complete
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: CALHOUN G M; SIPS D C; SUFFERN E S
Patent Family (1 patents, 1 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 6529945	B1	20030304	US 1999361079	A	19990726	200333	B

Priority Applications (no., kind, date): US 1999361079 A 19990726

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
US 6529945	B1	EN	16	8	

Original Titles:Data buffer management between two different systems Alerting Abstract ...ADVANTAGE - Provides multiple state machine design to efficiently service buffer updates from multiple sources and maintain dual buffer structures efficiently. Provides perfect mapping between the two different control block structures and achieves high speed full duplex data operation... Original Publication Data by AuthorityOriginal Abstracts:A data buffer management system and method between two different types of systems, The data buffer management system employs circular buffer chaining, wherein multiple state machines service buffer updates from multiple sources, dual buffer structures are maintained, mapping is provided between two different control block structures, and full duplex operation is supported. The data buffer management system... ... is performed by transferring and storing data from one of the two different systems to the data buffer memory The data in the data buffer memory is converted and read by another of the two different systems. A... ... performed by transferring and storing data from the other of the two different systems to the data buffer memory. >...Claims:the first system to the data buffer memory to be converted and read by the second system,transferring and storing data from the second system to the data buffer memory,allowing the data transferred from the second system to the data buffer memory to be... ... data from the first and second systems includes multiplexing and managing transfer and storage of the data into the data buffer memory, said multiplexing and managing comprising dividing usage of the data buffer memory by:coupling a first communication system to the first system and coupling a second communication system to the second system, wherein the second communication system includes a transmit enqueue, a descriptor processor, a first-in first-out buffer, a protocol engine, and a status processor,dividing the data buffer memory into a frame... ... status data, andwherein said transferring and storing data from the first system to the data buffer memory further includes:sending a data frame from the one of the two different systems to... ... descriptor format by providing descriptor format information for translating and converting between the first communication system and the second communication system,storing the descriptor format information into the descriptors block,writing to the transmit... ... frame from the descriptors block,using the descriptor processor for advising the first-in first-out buffer that the data frame is ready to be transferred and converted, for initiating transfer and... ... status block,freeing up the control block for the first communication system within the frame buffer block,updating an end pointer within the frame buffer block for the first communication system when the transfer status is recognized as a transfer... Basic Derwent Week: 200333...

8/3,K/2 (Item 2 from file: 350) Links
Fulltext available through: Order File History
Derwent WPIX

0010639909 & & *Drawing available*
WPI Acc no: 2001-247287/200126
XRPX Acc No: N2001-176144
Low latency network with synchronism between a sending application running on a first computer and a receiving application running on a second computer
Patent Assignee: AT & T INVESTMENTS UK INC (AMTT); AT & T LAB CAMBRIDGE LTD (AMTT)
Inventor: HODGES S J; MAPP G E; POPE S L; ROBERTS D E
Patent Family (10 patents, 20 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
GB 2349717	A	20001108	GB 199910280	A	19990504	200126	B
WO 2000067131	A2	20001109	WO 2000GB1691	A	20000503	200126	E
EP 1190317	A2	20020327	EP 2000925509	A	20000503	200229	E

			WO 2000GB1691	A	20000503		
EP 1302853	A2	20030416	EP 2000925509	A	20000503	200328	E
			EP 2002102564	A	20000503		
EP 1302854	A2	20030416	EP 2000925509	A	20000503	200328	E
			EP 2002102565	A	20000503		
EP 1302855	A2	20030416	EP 2000925509	A	20000503	200328	E
			EP 2002102567	A	20000503		
EP 1338965	A2	20030827	EP 2000925509	A	20000503	200357	E
			EP 2002102568	A	20000503		
US 20050289238	A1	20051229	WO 2000GB1691	A	20000503	200603	NCE
			US 2002980539	A	20020513		
			US 2005198260	A	20050805		
US 20060029053	A1	20060209	WO 2000GB1691	A	20000503	200612	NCE
			US 2002980539	A	20020513		
			US 2005198252	A	20050805		
US 20060034275	A1	20060216	US 2002980539	A	20020513	200614	NCE
			US 2005198043	A	20050805		

Priority Applications (no., kind, date): GB 199910280 A 19990504; WO 2000GB1691 A 20000503; US 2005198043 A 20050805; US 2005198252 A 20050805; US 2005198260 A 20050805

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
GB 2349717	A	EN	90	15		
WO 2000067131	A2	EN				
National Designated States,Original	US					
Regional Designated States,Original	AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE					
EP 1190317	A2	EN			PCT Application	WO 2000GB1691
					Based on OPI patent	WO 2000067131
Regional Designated States,Original	AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE					
EP 1302853	A2	EN			Division of application	EP 2000925509
					Division of patent	EP 1190317
Regional Designated States,Original	DE FR GB					
EP 1302854	A2	EN			Division of application	EP 2000925509
					Division of patent	EP 1190317
Regional Designated States,Original	DE FR GB					
EP 1302855	A2	EN			Division of application	EP 2000925509
					Division of patent	EP 1190317
Regional Designated States,Original	DE FR GB					
EP 1338965	A2	EN			Division of application	EP 2000925509
					Division of patent	EP 1190317
Regional Designated States,Original	DE FR GB					
US 20050289238	A1	EN			Division of application	WO 2000GB1691
					Division of application	US 2002980539
US 20060029053	A1	EN			Division of application	WO 2000GB1691
					Division of application	US 2002980539
US 20060034275	A1	EN			Division of application	US 2002980539

Original Publication Data by Authority...Claims:server application to the client application, both computers having a main memory and a memory mapped network interface, the method comprising the steps of:(A) providing a buffer in the main memory of each computer;(B) the client application, providing software stubs which produce a marshalled stream... computer for storing data being transferred as well as data identifying one or more pointer memory location(s);storing at said pointer memory location(s) at least one write pointer and at least one read pointer for indicating those areas of the buffer available for... ... update the indication of the area(s) of the buffer available for reads and the area(s) available for writes;in dependence on the values of WRP(s) and RDP(s), the receiver application reading from the buffer; andupdating the value of the RDP(s), after a read has taken place, to update the indication of the area... ... Basic Derwent Week: 200126...

8/3,K/3 (Item 3 from file: 350) Links
Fulltext available through: Order File History
Derwent WPIX

0009591541 & & *Drawing available*
WPI Acc no: 1999-539807/199945
XRPX Acc No: N1999-400003
Performance increasing method for multi-processor computer system
Patent Assignee: DATA GENERAL CORP (DATG)
Inventor: KIMMEL J S
Patent Family (1 patents, 1 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 5956754	A	19990921	US 1997796651	A	19970303	199945	B

Priority Applications (no., kind, date): US 1997796651 A 19970303

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
US 5956754	A	EN	26	8	

...NOVELTY - A selected shared pointer is checked to be null and if so, a buffer pointer is invalidated using an available slot. The selected shared pointer is set to point to... Original Publication Data by Authority...Claims:user tasks and each of said slots being in either one of a plurality of mapped states, the unmapped state or the remapping state; (e) a plurality of buffers each one of said buffers being a piece of said large data object and capable of being shared by at least two of said user tasks; (f) a plurality of shared pointers... ... said buffers; said method comprising responding to a call to a library function to map a selected one of said shared pointers to its corresponding shared buffer by: (I) checking to see if said selected shared pointer is null and if it is null performing the following substeps: (i) locating an available slot in said mapping table; (ii) placing said available slot into the remapping state; (iii)invalidating any buffer pointer which is using said available slot; (iv) placing said available slot into the mapped state; (v) invalidating any TLB entries on the executing CPU corresponding to said available slot; (vi) setting said selected shared pointer to point to said... ... Basic Derwent Week: 199945...

8/3,K/4 (Item 4 from file: 350) Links
Fulltext available through: Order File History
Derwent WPIX

0009463691 & & *Drawing available*
WPI Acc no: 1999-404015/199934
XRPX Acc No: N1999-301053
Asynchronous transfer mode cell interface unit for high speed transmission of digital codes, video and voice in communication network
Patent Assignee: LSI LOGIC CORP (LSIL-N)
Inventor: DANIEL T; NATTKEMPER D; VARMA S
Patent Family (1 patents, 1 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 5920561	A	19990706	US 1996614806	A	19960307	199934	B

Priority Applications (no., kind, date): US 1996614806 A 19960307

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
US 5920561	A	EN	37	17	

Alerting Abstract ...ATM data cells for storage in the respective memory segments, each of which includes a pointer, to either another memory segment containing the successive ATM data cell segment or to a null address, thus creating... Original Publication Data by Authority...Original Abstracts:repetitive data manipulation tasks, while these tasks are performed by one or more hardware-implemented coprocessors using memory mapped data structures and linked lists of data. ...Claims:said ATM data cells into segments for storage in respective segments of said memory, with each memory segment also including a pointer to either another memory segment containing a next-successive ATM data cell segment or to a null address thus creating a linked-list of memory segments each containing a respective ATM data cell segment and a pointer, and to reassemble the ATM data cells utilizing the memory addresses held in said registers as first element pointers and as last element pointers of the linked-list data structure.... Basic Derwent Week: 199934...

8/3,K/5 (Item 5 from file: 350) Links
Fulltext available through: Order File History
Derwent WPIX

0009114701 & & *Drawing available*
WPI Acc no: 1999-034419/199903

XRPX Acc No: N1999-025763
Interconnection and termination device for ATM communication system - maintains calendar based schedule table with pointers to memory locations of virtual connections of ATM communication system network, that is to be serviced in particular ATM time slot
Patent Assignee: LSI LOGIC CORP (LSIL-N)
Inventor: DANIEL T; NATTKEMPER D; VARMA S
Patent Family (1 patents, 1 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 5841772	A	19981124	US 1996612194	A	19960307	199903	B

Priority Applications (no., kind, date): US 1996612194 A 19960307

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
US 5841772	A	EN	38	17	

...maintains calendar based schedule table with pointers to memory locations of virtual connections of ATM communication system network, that is to be serviced in... Alerting Abstract ...a memory which receives and stores data cells and data structures of linked lists with memory address pointers as well as internal memory address pointers to successive elements of the linked list of data structures, in succession and regression. Using the memory address pointers a permanently preconfigured processor segments the ATM data cell that is finally reassembled in the... ...Timers are also included in a timer unit. A calendar based schedule table with pointers to memory locations of virtual connections of the ATM communication system network is maintained by a schedule... Original Publication Data by Authority...Original Abstracts:repetitive data manipulation tasks, while these tasks are performed by one or more hardware-implemented coprocessors using memory mapped data structures and linked lists of data. ...Claims:means for receiving, storing and recovering data cells, and data-structures of linked lists with memory address pointers to starting and ending memory addresses as well as internal memory address pointers to successive elements of said linked-list data structures by memory addresses in succession and regression;a permanently pre... ... to reassemble said segmented ATM data cells stored in said memory means, and using said memory address pointers to recover and reassemble said data cells;input/output (I/O) port interface means for communicating said device with an ATM... ... timers; anda scheduler unit including means for maintaining a calendar based schedule table with pointers to memory locations of virtual connections of said ATM communication system network to be serviced by said pre-configured processor in a particular ATM cell time slot;wherein said programmable processor... ... Basic Derwent Week: 199903...

8/3,K/6 (Item 6 from file: 350) Links
Fulltext available through: Order File History
Derwent WPIX

0008866699 & & *Drawing available*
WPI Acc no: 1998-414306/199835
XRPX Acc No: N1998-322421
Interleaved to planar conversion method for colour data arrays - involves three phases of cycles through data shuffling data around using algorithm to determine next element to be moved
Patent Assignee: ELECTRONICS FOR IMAGING (ELIM-N); ELECTRONICS IMAGING INC (ELIM-N)
Inventor: JACKSON B G; JACKSON G
Patent Family (12 patents, 69 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
WO 1998032090	A2	19980723	WO 1997US24152	A	19971219	199835	B
AU 199859049	A	19980807	AU 199859049	A	19971219	199901	E
US 5867179	A	19990202	US 1996775791	A	19961231	199912	E
BR 199714446	A	20000606	BR 199714446	A	19971219	200036	E
			WO 1997US24152	A	19971219		
EP 1025541	A2	20000809	EP 1997954650	A	19971219	200039	E
			WO 1997US24152	A	19971219		
AU 723974	B	20000907	AU 199859049	A	19971219	200048	E
NZ 336478	A	20001027	NZ 336478	A	19971219	200062	E
			WO 1997US24152	A	19971219		
US 6341017	B1	20020122	US 1996775791	A	19961231	200208	E
			US 1998181073	A	19981027		
JP 2002516049	W	20020528	WO 1997US24152	A	19971219	200238	E
			JP 1998534395	A	19971219		
EP 1025541	B1	20040915	EP 1997954650	A	19971219	200460	E
			WO 1997US24152	A	19971219		
DE 69730754	E	20041021	DE 69730754	A	19971219	200469	E
			EP 1997954650	A	19971219		
			WO 1997US24152	A	19971219		
DE 69730754	T2	20050929	DE 69730754	A	19971219	200568	E
			EP 1997954650	A	19971219		

			WO 1997US24152	A	19971219		

Priority Applications (no., kind, date): US 1996775791 A 19961231; US 1998181073 A 19981027

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
WO 1998032090	A2	EN	43	5		
National Designated States,Original	AL AU BA BB BG BR CA CN CU CZ EE GE HU ID IL IS JP KP KR LC LK LR LT LV MG MK MN MX NO NZ PL RO SG SI SK SL TR TT UA UZ VN YU					
Regional Designated States,Original	AT BE CH DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW					
AU 199859049	A	EN			Based on OPI patent	WO 1998032090
BR 199714446	A	PT			PCT Application	WO 1997US24152
					Based on OPI patent	WO 1998032090
EP 1025541	A2	EN			PCT Application	WO 1997US24152
					Based on OPI patent	WO 1998032090
Regional Designated States,Original	AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE					
AU 723974	B	EN			Previously issued patent	AU 9859049
					Based on OPI patent	WO 1998032090
NZ 336478	A	EN			PCT Application	WO 1997US24152
					Based on OPI patent	WO 1998032090
US 6341017	B1	EN			Continuation of application	US 1996775791
					Continuation of patent	US 5867179
JP 2002516049	W	JA	37		PCT Application	WO 1997US24152
					Based on OPI patent	WO 1998032090
EP 1025541	B1	EN			PCT Application	WO 1997US24152
					Based on OPI patent	WO 1998032090
Regional Designated States,Original	AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE					
DE 69730754	E	DE			Application	EP 1997954650
					PCT Application	WO 1997US24152
					Based on OPI patent	EP 1025541
					Based on OPI patent	WO 1998032090
DE 69730754	T2	DE			Application	EP 1997954650
					PCT Application	WO 1997US24152
					Based on OPI patent	EP 1025541
					Based on OPI patent	WO 1998032090

Original Publication Data by Authority...Claims:each address visited in the frame buffer that is within the predetermined number of addresses;mapping interleaved data to planar data along additional paths through the frame buffer during a second phase, each additional path beginning at an address that has not been mapped during the first phase, and setting a flag associated with each address visited in the frame buffer that is included within the predetermined number... ... number of pixels in the frame buffer, 4N = the number of bytes in said frame buffer, and Q = 4N-1... map cycle throughout a frame buffer during a first phase;finding additional map cycles and mapping through said frame buffer during a second phase;mapping all remaining cycles during a third phase; anditerating a function, C(i)=4(i-3N)+3, for 3N<=i<4N, that maps planar addresses to interleaved addresses;where i=index of a planar byte in said frame buffer; andwhere N=the number of pixels in said frame buffer and 4N=the number of bytes in said frame buffer... ... map cycle throughout a frame buffer during a first phase;finding additional map cycles and mapping through said frame buffer during a second phase;mapping all remaining cycles during a third phase;iterating a function, 4N, that maps planar addresses... Basic Derwent Week: 199835...

8/3,K/7 (Item 7 from file: 350) Links
Fulltext available through: Order File History
Derwent WPIX

0008719915 & & *Drawing available*
WPI Acc no: 1998-260844/199823
XRPX Acc No: N1998-205671
Computerised 3D graphical shadow display method - involves storing depth map containing sample values identifying distance from pixel location to light source allowing rendering of scene
Patent Assignee: SILICON GRAPHICS INC (SILI-N)
Inventor: FORAN J L; VAN WIDENFELT R A
Patent Family (1 patents, 1 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 5742749	A	19980421	US 199389799	A	19930709	199823	B
			US 1996603691	A	19960220		

Priority Applications (no., kind, date): US 199389799 A 19930709; US 1996603691 A 19960220

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
US 5742749	A	EN	20	8	Continuation of application	US 199389799

Original Publication Data by Authority...Original Abstracts:viewpoint of a light source using z-buffering to create a two dimensional depth map from said z-buffer; storing the depth map in texture mapping storage; rendering the scene from the viewpoint of the viewer; for every pixel in view creating an index info... ...Claims:using a projective texture mapping technique, said light system coordinates comprising a pixel depth map index for indexing said texture map storage and a pixel depth value;retrieving a predetermined number of depth map sample values from said texture map storage based on said pixel depth map index;comparing each of said predetermined... ... Basic Derwent Week: 199823...

8/3,K/8 (Item 8 from file: 350) Links
Fulltext available through: Order File History
Derwent WPIX

0007730835 & & *Drawing available*
WPI Acc no: 1996-354199/199635
XRPX Acc No: N1996-298749
Data processor with address translation capability - has execution unit coupled to address translation buffer using translation mapping fields with replacement pointer allowing overwriting of fields when necessary
Patent Assignee: MOTOROLA INC (MOTI)
Inventor: REININGER R; SLATON J
Patent Family (1 patents, 1 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 5539892	A	19960723	US 1994284953	A	19940802	199635	B

Priority Applications (no., kind, date): US 1994284953 A 19940802

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
US 5539892	A	EN	9	5	

Alerting Abstract ...state of a user-accessible control register during normal replacement operation of the address translation buffer. The replacement pointer field is operable to overwrite a second value to the replacement pointer field responsive to... Original Publication Data by Authority...Claims:generating an address;
an address translation buffer coupled to the execution unit, the
address translation buffer comprising a plurality of entries, each one of the plurality of entries comprising:
a set of N translation mapping fields, where N is an integer, a differing one of the set of N translation... ... a new translation mapping; and
a replacement pointer control unit coupled to the address translation buffer, the replacement pointer control unit operable to overwrite a first value to the replacement pointer field responsive to a first state of a user-accessible control register during normal replacement operation of the address translation buffer, the replacement pointer field operable to overwrite a second value to the replacement pointer field responsive to a second state of the user-accessible control register.... Basic Derwent Week: 199635...

8/3,K/9 (Item 9 from file: 350) Links
Fulltext available through: Order File History
Derwent WPIX

0007161847 & & *Drawing available*
WPI Acc no: 1995-200073/199526
XRPX Acc No: N1995-157186
Virtual addressing buffer circuit - compares input address to stored match address after filtering address bits not relevant to address match, and generates output address from translated address and original input address
Patent Assignee: AST RES INC (ASTR-N); SAMSUNG ELECTRONICS CO LTD (SMSU)
Inventor: KIM J S
Patent Family (10 patents, 21 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
WO 1995010084	A2	19950413	WO 1994US11273	A	19941004	199526	B
AU 199479286	A	19950501	AU 199479286	A	19941004	199532	E
US 5526503	A	19960611	US 1993132643	A	19931006	199629	E
WO 1995010084	A3	19960229	WO 1994US11273	A	19941004	199630	E
US 5737769	A	19980407	US 1993132643	A	19931006	199821	E
			US 1995520154	A	19950828		
			US 1997788938	A	19970124		

US 5809559	A	19980915	US 1993132643	A	19931006	199844	E
			US 1995457262	A	19950601		
			US 1997895737	A	19970717		
CA 2168335	C	20020730	CA 2168335	A	19941004	200259	E
			WO 1994US11273	A	19941004		
KR 341180	B	20021123	WO 1994US11273	A	19941004	200333	E
			KR 1996701782	A	19960404		
CA 2383750	C	20030701	CA 2168335	A	19941004	200350	E
			CA 2383750	A	19941004		
CA 2383747	C	20040914	CA 2168335	A	19941004	200461	E
			CA 2383747	A	19941004		

Priority Applications (no., kind, date): US 1993132643 A 19931006; US 1995457262 A 19950601; US 1995520154 A 19950828; US 1997788938 A 19970124; US 1997895737 A 19970717

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
WO 1995010084	A2	EN	50	5		
National Designated States,Original	AU CA CN JP KR					
Regional Designated States,Original	AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE					
AU 199479286	A	EN			Based on OPI patent	WO 1995010084
US 5526503	A	EN	17			
WO 1995010084	A3	EN				
US 5737769	A	EN	18	5	Division of application	US 1993132643
					Continuation of application	US 1995520154
					Division of patent	US 5526503
US 5809559	A	EN			Division of application	US 1993132643
					Continuation of application	US 1995457262
					Division of patent	US 5526503
CA 2168335	C	EN			PCT Application	WO 1994US11273
					Based on OPI patent	WO 1995010084
KR 341180	B	KO			PCT Application	WO 1994US11273
					Previously issued patent	KR 96705274
					Based on OPI patent	WO 1995010084
CA 2383750	C	EN			Division of application	CA 2168335
CA 2383747	C	EN			Division of application	CA 2168335

Original Publication Data by Authority...Original Abstracts:terminate command is provided to a bus controller connected to the CPU and a local memory when the match indicator is active. An interrupt sent to the CPU from the bus controller in response to the terminate command interrupts the CPU. An interrupt routine triggered by the CPU interruption... ... in local memory to a memory status buffer. Upon completion of the interrupt routine, a second virtual addressing buffer circuit copies the emulated data stored in the local memory status buffer to the CPU so that it appears that the emulated device responded... ...Claims:to a slower downstream bus where a requested peripheral device is located; andutilizing a second programmable buffer address circuit, said second programmable buffer address circuit having at least a second writable memory element configured to store second address mapping data, to changeably redirect address requests for memory locations above the physical memory space according... ... in response to said interrupt signal, said interrupt routine copying emulated data stored in local memory to a status buffer; anda second virtual addressing buffer circuit, said second virtual address buffer copying said emulated data stored in said status buffer to said CPU.... Basic Derwent Week: 199526...

8/3,K/10 (Item 10 from file: 350) Links
Fulltext available through: Order File History
Derwent WPIX

0006687565 & & *Drawing available*
WPI Acc no: 1994-067590/199409
XRPX Acc No: N1994-052911
Data processor for maintenance of cache coherency - in multi-master computer system in which bus arbitration signals either are not available to the cache or are not exclusively relied upon
Patent Assignee: CYRIX CORP (CYRI-N)
Inventor: BRIGHTMAN T B; PATTON W C; SELGAS T D
Patent Family (2 patents, 10 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
EP 585117	A1	19940302	EP 1993306752	A	19930825	199409	B
US 5724549	A	19980303	US 1992864399	A	19920406	199816	E

			US 1992935564	A	19920826		
			US 1993131043	A	19931001		

Priority Applications (no., kind, date): US 1993131043 A 19931001; US 1992864399 A 19920406; US 1992935564 A 19920826

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
EP 585117	A1	EN	20	4		
Regional Designated States,Original	CH DE ES FR GB IE IT LI NL					
US 5724549	A	EN	18		C-I-P of application	US 1992864399
					Continuation of application	US 1992935564

Original Publication Data by Authority...Original Abstracts:by the microprocessor to I/O address space, except for those directed to a hard disk or an external coprocessor. If the bus architecture uses memory-mapped I/O, accesses by the microprocessor to selected regions of memory-mapped I/O space could also be used. The cache coherency functionality could alternatively be implemented... ... read/write accesses to I/O address space, except for those directed to a hard disk or an external coprocessor. If the bus architecture uses memory-mapped I/O, accesses to selected regions of memory-mapped I/O space could also be used. The cache coherency functionality could be implemented on-board the microprocessor. ...Claims:execution unit operably coupled with a buffer including addressable data storage locations accessible by said execution unit, and a detector coupled to said processor to detect signals generated by said processor representing at least one... ... ...

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